1. Features

The KNX6610A is the highest performance trench N-ch MOSFETS with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KNX6610A meet the RoHS and green product requirement, 100% EAS guaranteed with full function reliability approved.

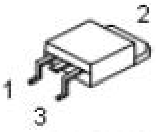
2. Features

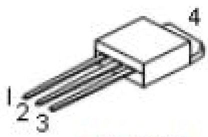
- $R_{DS(ON)}$=70mΩ(typ.)@V_{GS}=10V
- Advanced high cell density trench technology
- Super low gate charge
- Excellent Cdv/dt effect desline
- Green device available

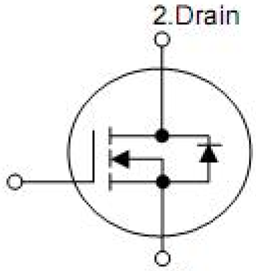
3. Applications

- High frequency point-of-load synchronous buck converter
- Networking DC-DC power system
- Load switch

4.Symbol







Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KND6610A	TO-252	KIA
KNU6610A	TO-251	KIA

5. Absolute maximum ratings

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current , V_{GS}@10V [1]	T_C=25°C	I_D	15	A
	T_C=100°C		8.5	
Pulsed drain current[2]		I_{DM}	24	
Power dissipation[3]	T_C=25°C	P_D	34.7	W
	T_A=25°C		2	
Single pulse avalanche engergy [3]		E_{AS}	7.3	mJ
Avalanche current		I_{AS}	11	A
Operating junction and storage temperature range		T_J ,T_{STG}	-55 to150	ºC

6. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance junction-case	$R_{\theta JC}$	-	3.6	ºC/W
Thermal resistance junction-ambient	$R_{\theta JA}$	-	62	

7. Electrical characteristics

(T_J=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	100	-	-	V
BV_{DSS} temperature coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference 25℃ I_D=1mA	-	0.098	-	V/ºC
Drain-source on-resistance[2]	$R_{DS(on)}$	V_{GS}=10V,I_D=8A	-	70	80	mΩ
		V_{GS}=4.5V,I_D=6A	-	80	100	
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}= V_{GS},I_D=250uA	1.0	1.5	2.5	V
$V_{GS(TH)}$ temperature coefficient	$\triangle V_{GS(TH)}$		-	-4.57	-	mV/ºC
Drain-source leakage current	I_{DSS}	V_{DS}=80V, V_{GS}=0V T_J=25°C	-	-	1	μA
		V_{DS}=80V, V_{GS}=0V T_J=55°C	-	-	5	
Gate-source forward leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Forward transconductance	gfs	V_{DS}=5V, I_D=10A	-	13	-	S
Gate resistance	R_g	V_{DS}=0V, V_{GS}=0V f=1MHz	1.2	1.8	3.5	Ω
Total gate charge(10V)	Q_g	V_{DS}=80V, I_D=10A V_{GS}=10V	-	26.2		nC
Gate-source charge	Q_{gs}		-	4.6		
Gate-drain charge	Q_{gd}		-	5.1		
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, I_D=10A, R_G=3.3Ω,V_{GS}=10V	-	4.2		ns
Rise time	t_r		-	8.2		
Turn-off delay time	$t_{d(off)}$		-	35.6		
Fall time	t_f		-	9.6		
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz	-	1220		pF
Output capacitance	C_{oss}		-	250		
Reverse transfer capacitance	C_{rss}		-	140		
Single pulse avalanche energy[5]	EAS	V_{DD}=25V,I_{AS}=5A L=0.1mH	1.5	-	-	mJ
Continuous source current[1,6]	I_S	V_D=V_G=0V, Force current	-	-	15	A
Maximum pulsed current[2,6]	I_{SM}		-	-	24	
Diode forward voltage[2]	V_{SD}	I_S=1A, V_{GS}=0V T_J=25°C	-	-	1.2	V
Reverse recovery time	t_{rr}	I_F=10A,dI/dt=100A/μs T_J=25°C	-	37	-	ns
Reverse recovery charge	Q_{rr}		-	27.3	-	nC

Note:

1. The data tested by surface mounted on a 1 inch^2 board with 2OZ copper.
2. The data tested by pulsed, pulse width≤ 300μs, duty cycle ≤ 2%.
3. The EAS data shows max. rating. The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH, I_{AS}=11A
4. The power dissipation is limited by 150 ºC junction temperature.
5. The min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

8. Typical operating characteristics

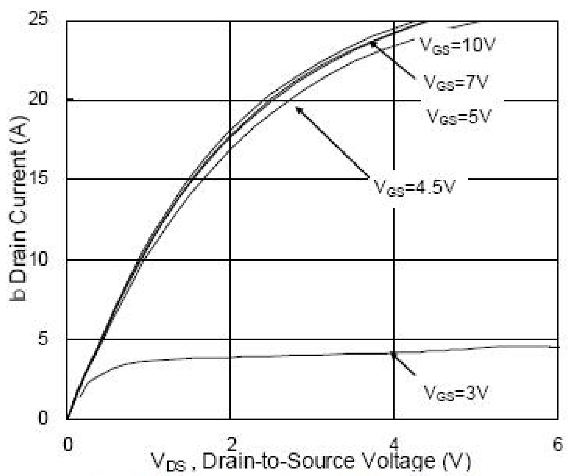


Fig.1 Typical output characteristics

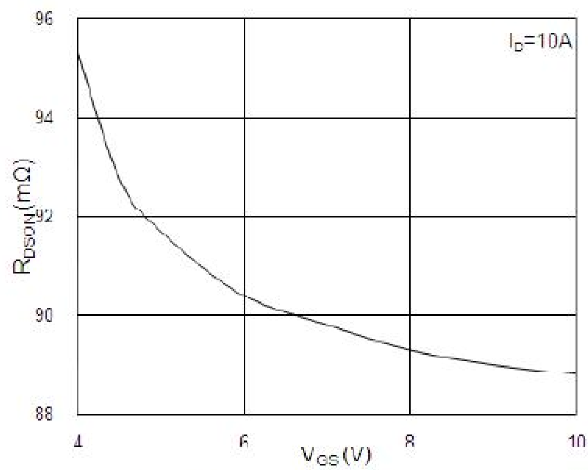


Fig.2 On-resistance vs. Gate-source

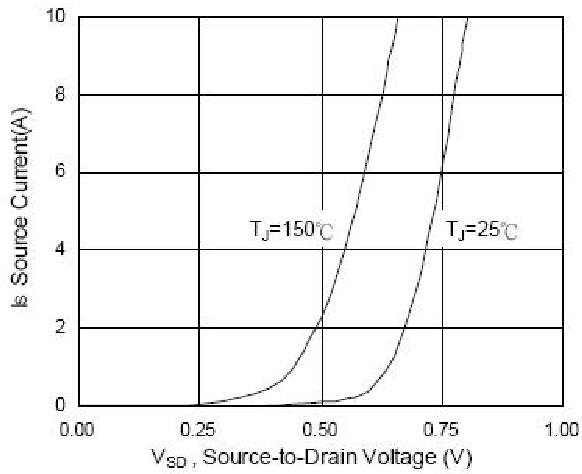


Fig.3 Forward characteristics of reverse

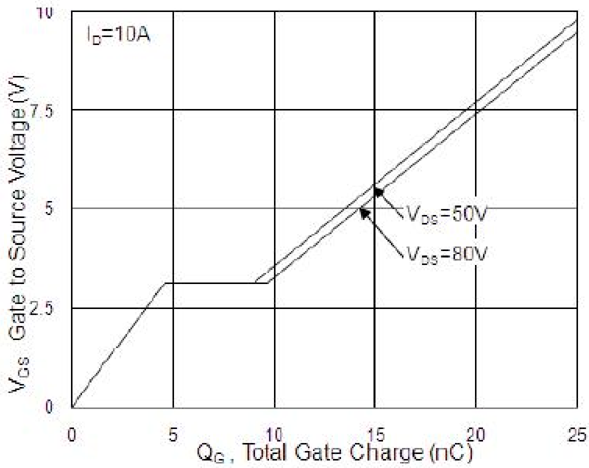


Fig.4 Gate-charge characteristics

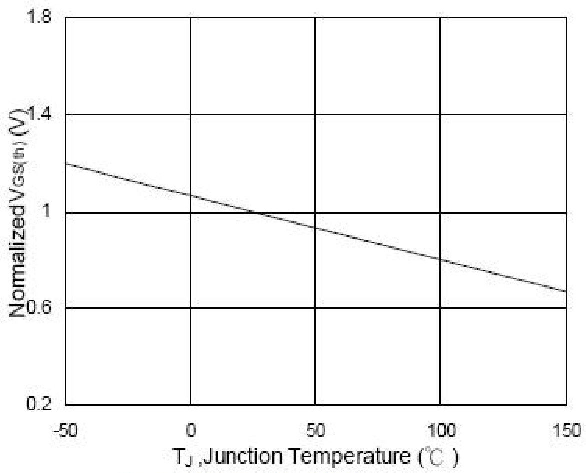


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

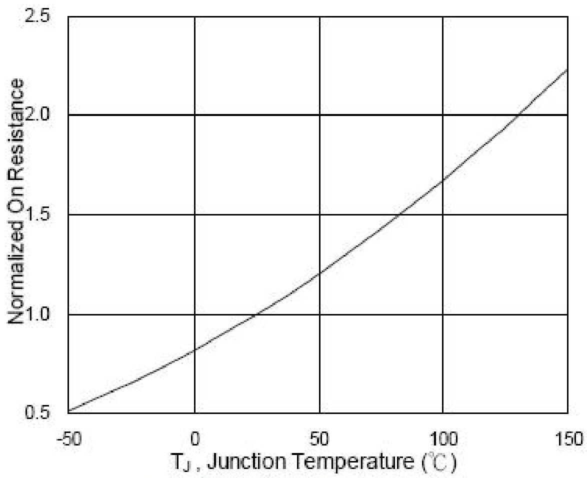


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

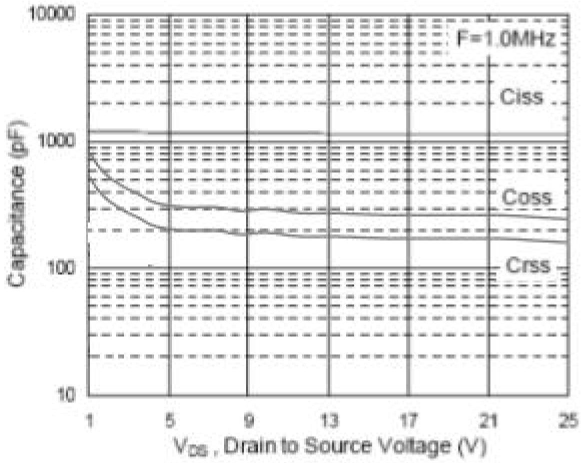


Fig.7 Capacitance

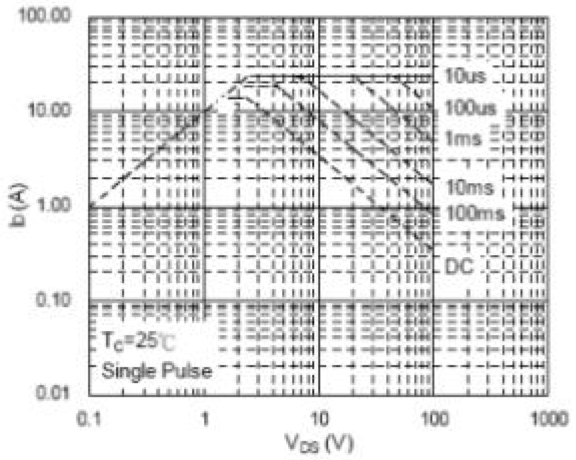


Fig.8 Safe operating area

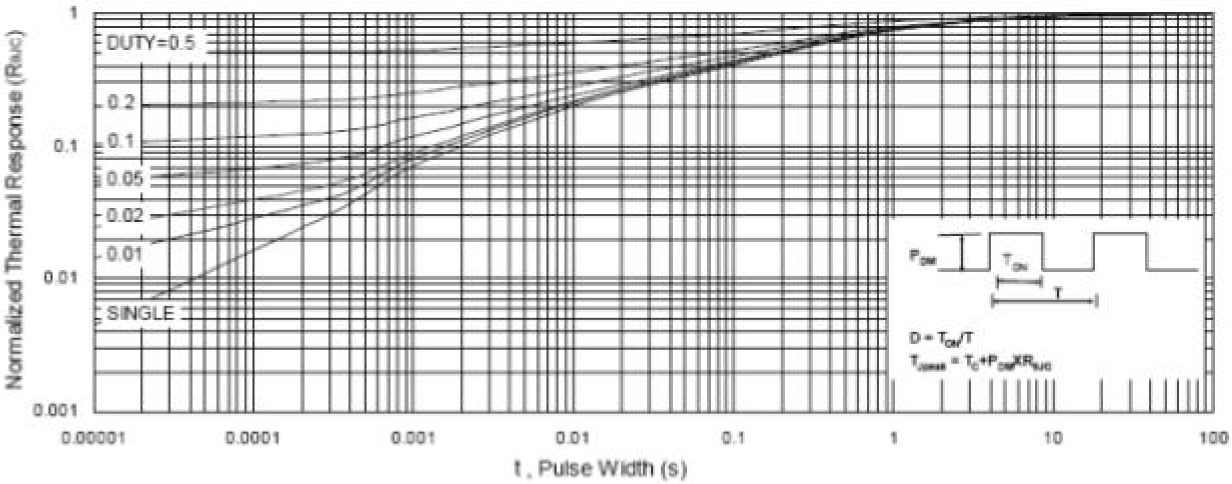


Fig.9 Normalized maximum transient thermal impedance

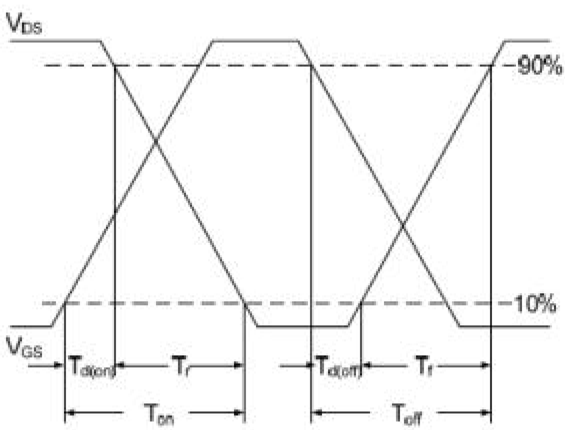


Fig.10 Switching time waveform

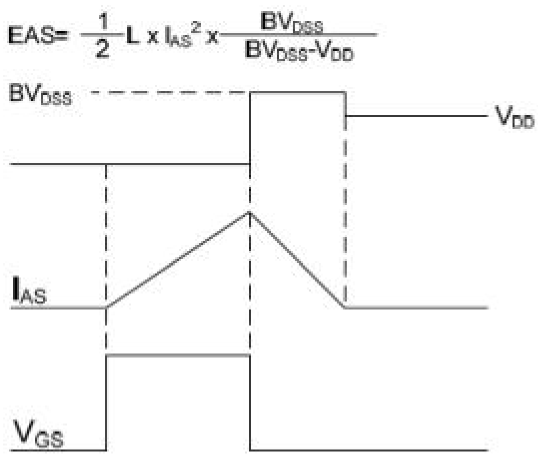


Fig.11 Gate charge waveform